Micropower, OVP, Rail-to-Rail Input/Output Operational Amplifier

ADA4091-2/ADA4091-4

FEATURES

Single-supply operation: 2.7 V to 36 V
Wide input voltage range
Rail-to-rail output swing
Low supply current: 200 µA/amplifier
Wide bandwidth: 1.2 MHz
Slew rate: 0.46 V/µs
Low offset voltage: 250 µV maximum
No phase reversal
Overvoltage protection (OVP)
  25 V above/below supply rails at ±5 V
  12 V above/below supply rails at ±15 V

APPLICATIONS

Industrial process control
Battery-powered instrumentation
Power supply control and protection
Telecommunications
Remote sensors
Low voltage strain gage amplifiers
DAC output amplifiers

GENERAL DESCRIPTION

The ADA4091-2 dual and ADA4091-4 quad are micropower, single-supply, 1.2 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from a +2.7 V to +30 V single supply as well as from ±1.35 V to ±15 V dual supplies.

The ADA4091 family features a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection, or OVP.

Applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers, for example, to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios (SNR).

The ADA4091 family is specified over the extended industrial temperature range of −40°C to +125°C. The ADA4091 family is part of the growing selection of 36 V, low power op amps from Analog Devices, Inc., (see Table 1).

PIN CONFIGURATIONS

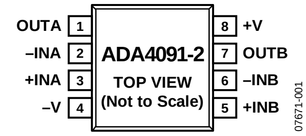

Figure 1. 8-Lead, Narrow-Body SOIC (R-8)

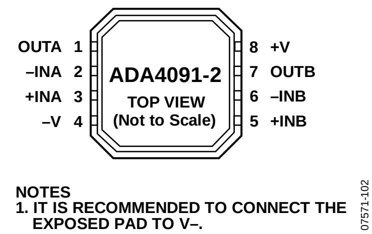

Figure 2. 8-Lead LFCSP (CP-8-9)

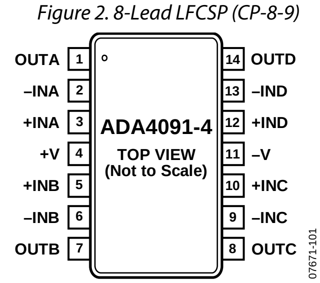

Figure 3. 14-Lead TSSOP (RU-14)

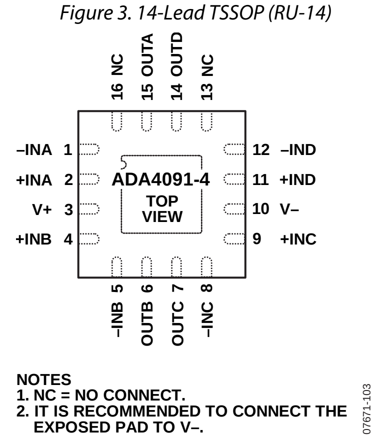

Figure 4. 16-Lead LFCSP (CP-16-17)

The ADA4091-2 is available in 8-lead, plastic SOIC and 8-lead LFCSP packages. The ADA4091-4 is available in 14–lead TSSOP and 16-lead LFCSP surface-mount packages.

Table 1. Low Power, 36 V Operational Amplifiers

Family	Rail-to-Rail I/O	PJFET	Low Noise
Single			OP1177
Dual	ADA4091-2	AD8682	OP2177
Quad	ADA4091-4	AD8684	OP4177

Rev. D

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{SY} = ±1.5 V, V_{CM} = 0.0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−250	−40	+250	µV
		LFCSP package only	−400	−40	+400	µV
		−40°C ≤ T_A ≤ +125°C	−600		+600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.5		µV/°C
Input Bias Current	I_B		−55	−44		nA
		−40°C ≤ T_A ≤ +85°C	−55		+55	nA
		−40°C ≤ T_A ≤ +125°C	−275		+275	nA
Input Offset Current	I_{OS}		−3	0.5	+3	nA
		−40°C ≤ T_A ≤ +85°C	−5		+5	nA
		−40°C ≤ T_A ≤ +125°C	−75		+75	nA
Input Voltage Range			−1.5		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −1.35 V to +1.35 V	84	100		dB
		−40°C ≤ T_A ≤ +125°C	78			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = −1.2 V to +1.2 V	106	113		dB
		−40°C ≤ T_A ≤ +125°C	101			dB
		R_L = 10 kΩ, V_O = −1.2 V to +1.2 V	92	94		dB
		−40°C ≤ T_A ≤ +125°C	85			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	1.490	1.495		V
		−40°C ≤ T_A ≤ +125°C	1.490			V
		R_L = 10 kΩ to GND	1.475	1.485		V
		−40°C to +125°C	1.455			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−1.499	−1.495	V
		−40°C ≤ T_A ≤ +125°C			−1.495	V
		R_L = 10 kΩ to GND		−1.495	−1.490	V
		−40°C ≤ T_A ≤ +125°C			−1.490	V
Short-Circuit Limit	I_{SC}	Source/sink		±31		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		102		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	108	126		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		165	200	µA
		−40°C ≤ T_A ≤ +125°C			300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.46		V/µs
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			1.22		MHz
Phase Margin	Φ_M			69		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		24		nV/√Hz

V_{SY} = ±5.0 V, V_{CM} = 0.0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−250	−45	+250	µV
		LFCSP package only	−400	−40	+400	µV
		−40°C ≤ T_A ≤ +125°C	−600		+600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.5		µV/°C
Input Bias Current	I_B		−60	−50		nA
		−40°C ≤ T_A ≤ +85°C	−80		+80	nA
		−40°C ≤ T_A ≤ +125°C	−350		+350	nA
Input Offset Current	I_{OS}		−3	0.5	+3	nA
		−40°C ≤ T_A ≤ +85°C	−7		+7	nA
		−40°C ≤ T_A ≤ +125°C	−100		+100	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −4.85 V to +4.85 V	95	113		dB
		−40°C ≤ T_A ≤ +125°C	88			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = ±4.7 V	113	117		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
		R_L = 10 kΩ, V_O = ±4.7 V	98	100		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.980	4.990		V
		−40°C ≤ T_A ≤ +125°C	4.980			V
		R_L = 10 kΩ to GND	4.950	4.960		V
		−40°C ≤ T_A ≤ +125°C	4.900			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−4.998	−4.990	V
		−40°C ≤ T_A ≤ +125°C			−4.980	V
		R_L = 10 kΩ to GND		−4.990	−4.980	V
		−40°C ≤ T_A ≤ +125°C			−4.975	V
Short-Circuit Limit	I_{SC}	Source/sink		±20		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		77		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	108	126		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		180	225	µA
		−40°C ≤ T_A ≤ +125°C			300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.46		V/µs
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			1.22		MHz
Phase Margin	Φ_M			70		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		24		nV/√Hz

V_{SY} = ±15.0 V, V_{CM} = 0.0 V, V_O = 0.0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−250	−35	+250	µV
		LFCSP package only	−400	−40	+400	µV
		−40°C ≤ T_A ≤ +125°C	−600		+600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.0		µV/°C
Input Bias Current	I_B		−60	−50		nA
		−40°C ≤ T_A ≤ +85°C	−80		+80	nA
		−40°C ≤ T_A ≤ +125°C	−510		+510	nA
Input Offset Current	I_{OS}		−3	0.5	+3	nA
		−40°C ≤ T_A ≤ +85°C	−10		+10	nA
		−40°C ≤ T_A ≤ +125°C	−140		+140	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −14.85 V to +14.85 V	104	121		dB
		−40°C ≤ T_A ≤ +125°C	95			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = ±14.7 V	116	119		dB
		−40°C ≤ T_A ≤ +125°C	108			dB
		R_L = 10 kΩ, V_O = ±14.7 V	102	104		dB
		−40°C ≤ T_A ≤ +125°C	93			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	14.975	14.980		V
		−40°C ≤ T_A ≤ +125°C	14.950			V
		R_L = 10 kΩ to GND	14.900	14.920		V
		−40°C ≤ T_A ≤ +125°C	14.800			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−14.996	−14.990	V
		−40°C ≤ T_A ≤ +125°C			−14.985	V
		R_L = 10 kΩ to GND		−14.975	−14.950	V
		−40°C ≤ T_A ≤ +125°C			−14.940	V
Short-Circuit Limit	I_{SC}	Source/sink		±20		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		71		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	108	126		dB
		−40°C ≤ T_A ≤ +125°C	100			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		200	250	µA
		−40°C ≤ T_A ≤ +125°C			350	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.46		V/µs
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			1.27		MHz
Phase Margin	Φ_M			72		Degrees
Channel Separation	CS	f = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		25		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	Refer to the Input Overvoltage Protection section
Differential Input Voltage[1]	±V_{SY}
Input Current	±5 mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Input current should be limited to ±5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

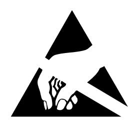
THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard PCB with zero airflow. The exposed pad is soldered to the application board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	155	45	°C/W
14-Lead TSSOP (RU-14)	112	35	°C/W
8-Lead LFCSP (CP-8-9)	75	12	°C/W
16-Lead LFCSP (CP-16-17)	55	14	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

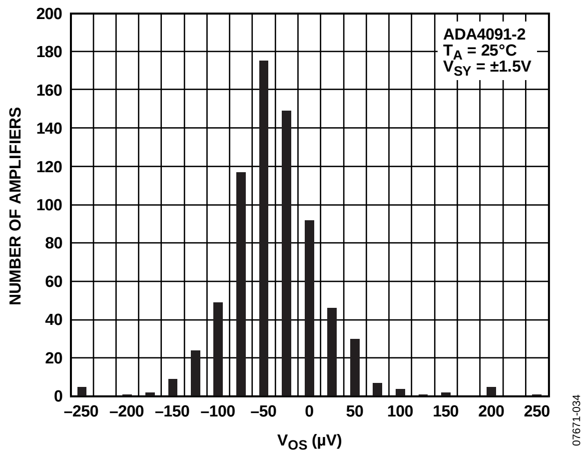


Figure 5. Input Offset Voltage Distribution

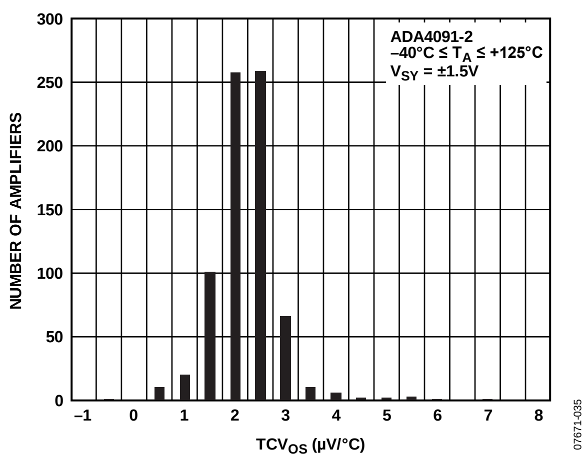


Figure 6. TCV_{OS} Distribution

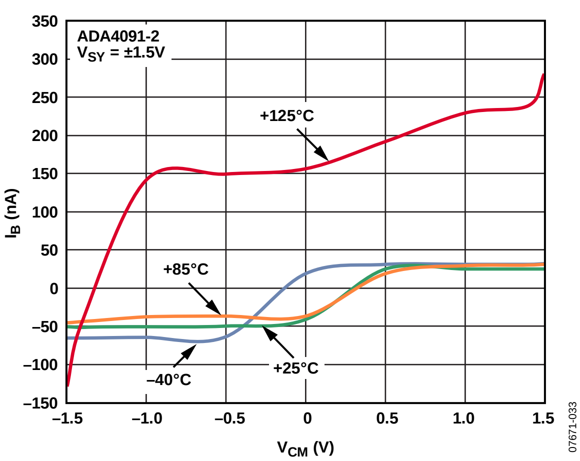


Figure 7. Input Bias Current vs. Common-Mode Voltage

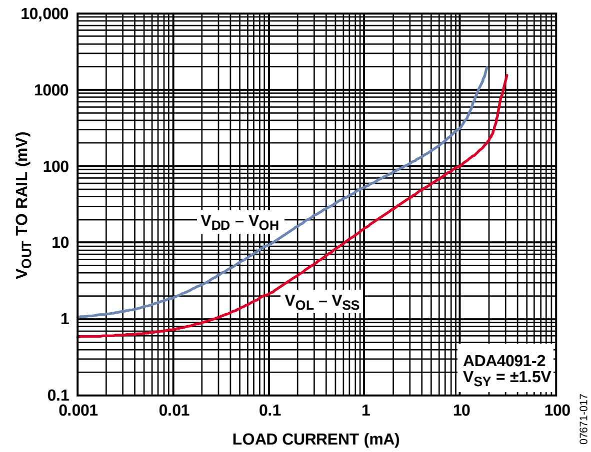


Figure 8. Dropout Voltage vs. Load Current

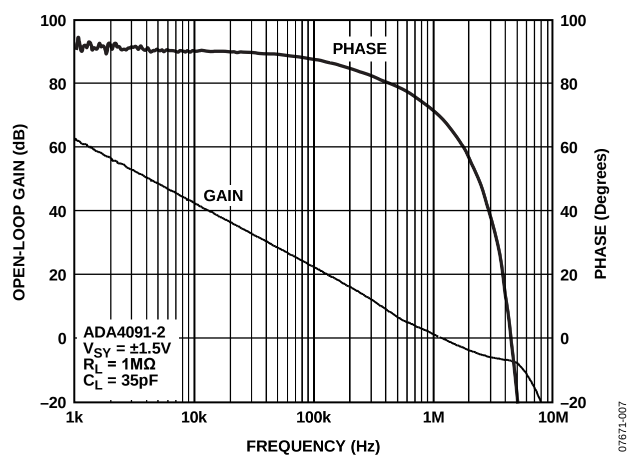


Figure 9. Open-Loop Gain and Phase vs. Frequency

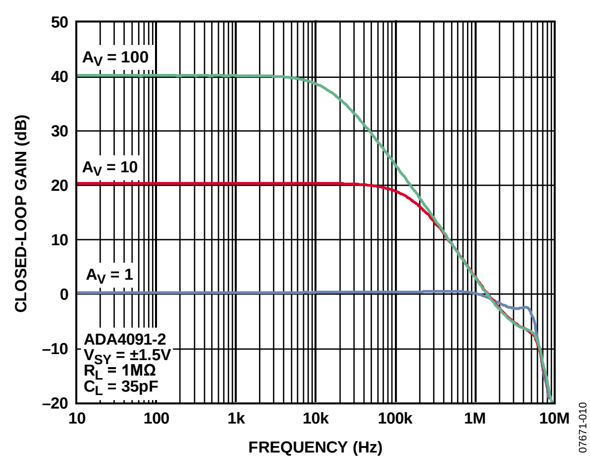


Figure 10. Closed-Loop Gain vs. Frequency

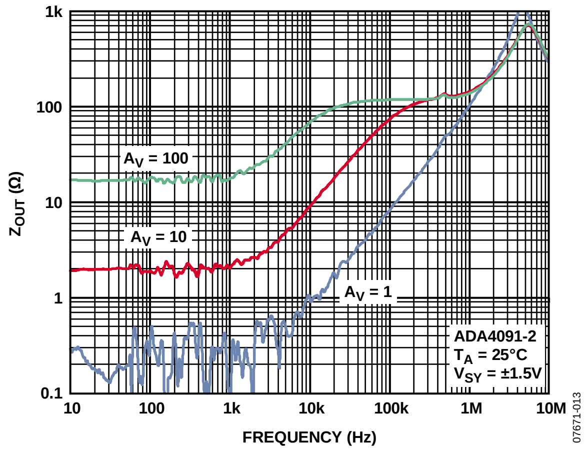


Figure 11. Output Impedance vs. Frequency

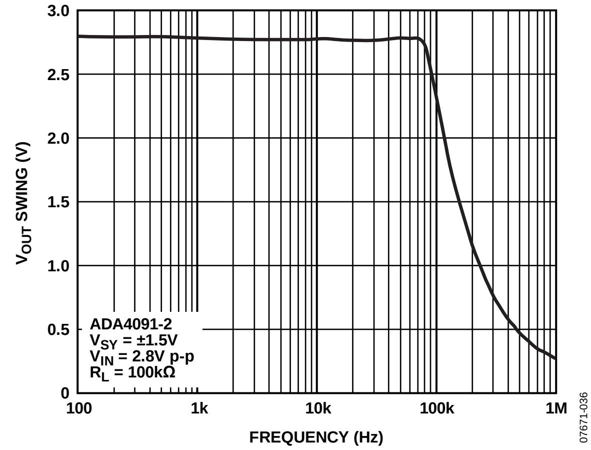


Figure 14. Output Swing vs. Frequency

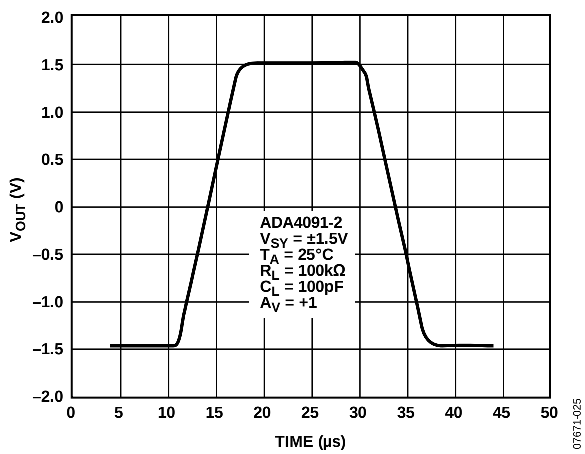


Figure 12. Large Signal Transient Response

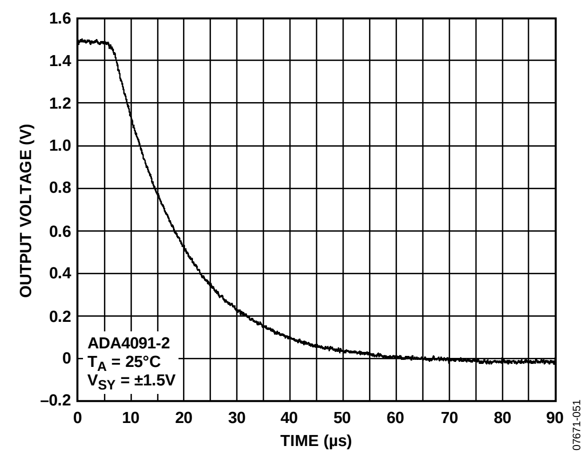


Figure 15. Positive Overload Recovery

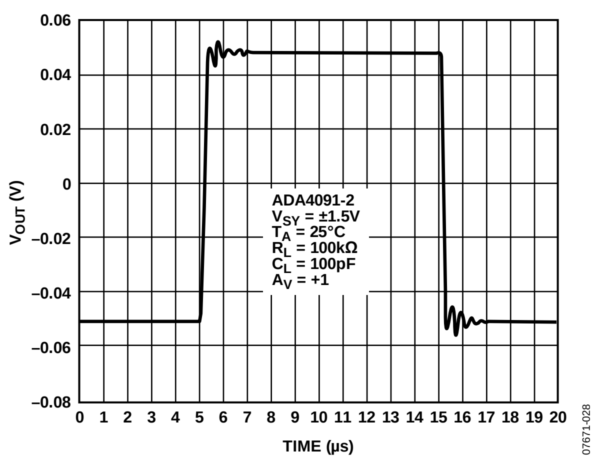


Figure 13. Small Signal Transient Response

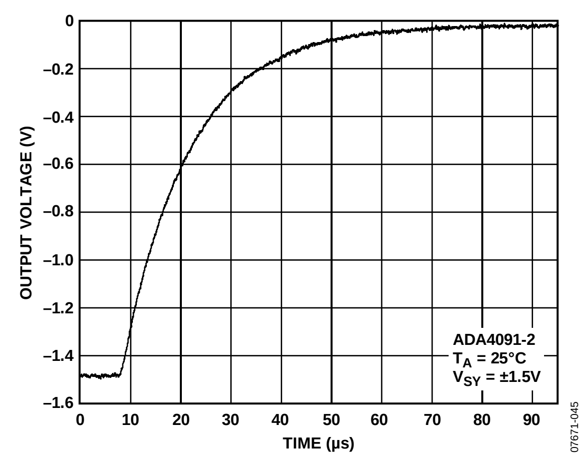


Figure 16. Negative Overload Recovery

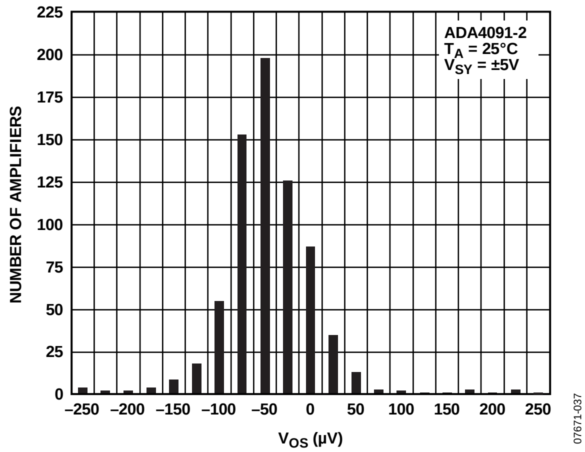


Figure 17. Input Offset Voltage Distribution

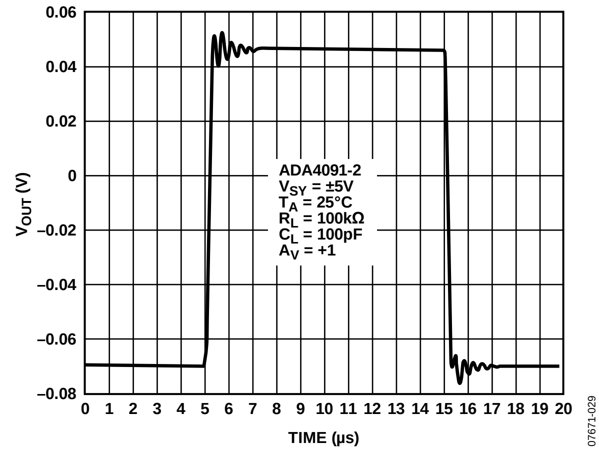


Figure 20. Small Signal Transient Response

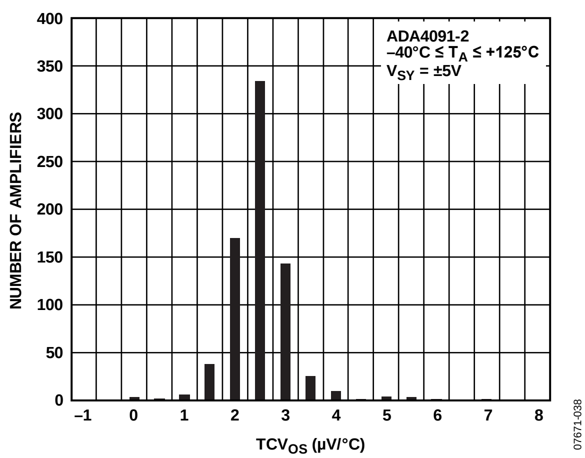


Figure 18. TCV_{OS} Distribution

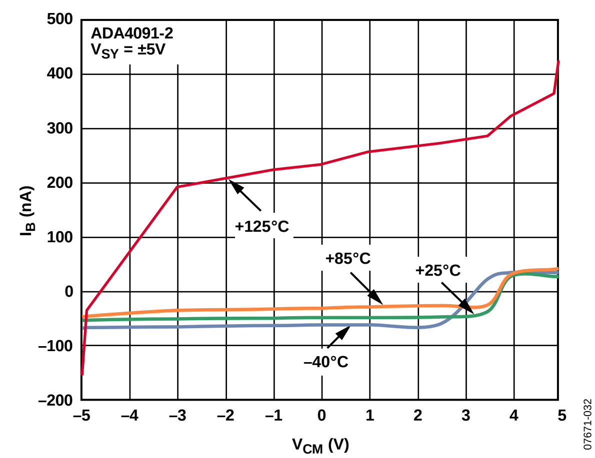


Figure 21. Input Bias Current vs. Common-Mode Voltage

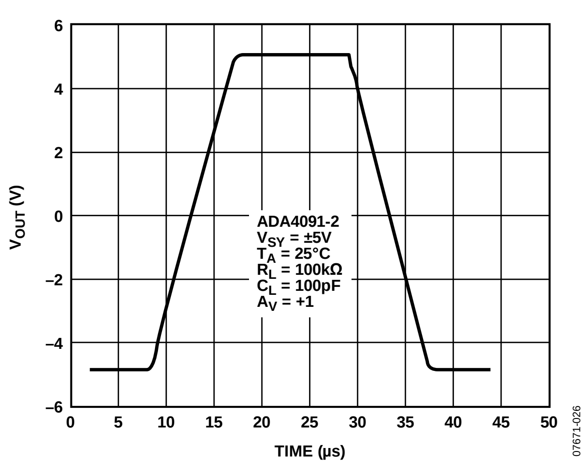


Figure 19. Large Signal Transient Response

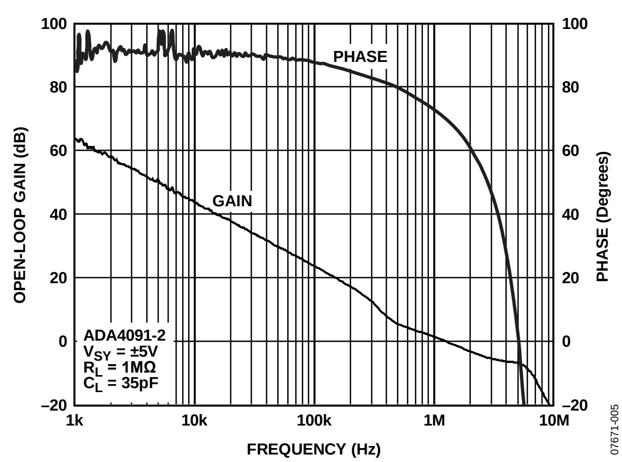


Figure 22. Open-Loop Gain and Phase vs. Frequency

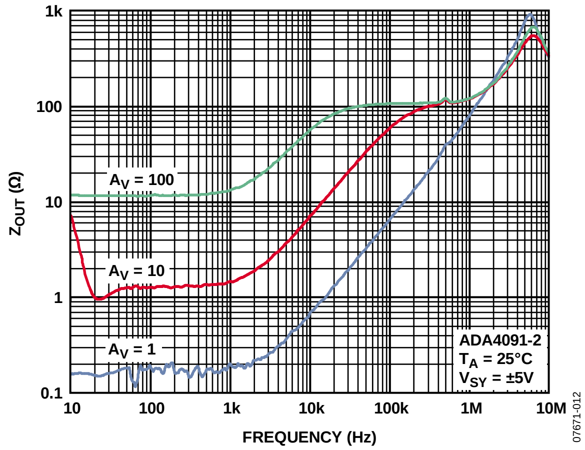


Figure 23. Output Impedance vs. Frequency

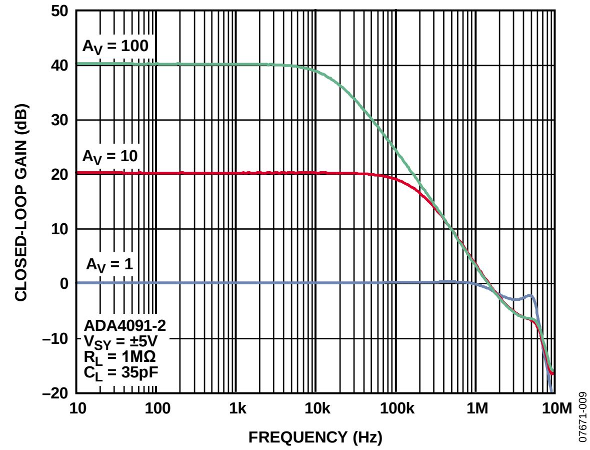


Figure 26. Closed-Loop Gain vs. Frequency

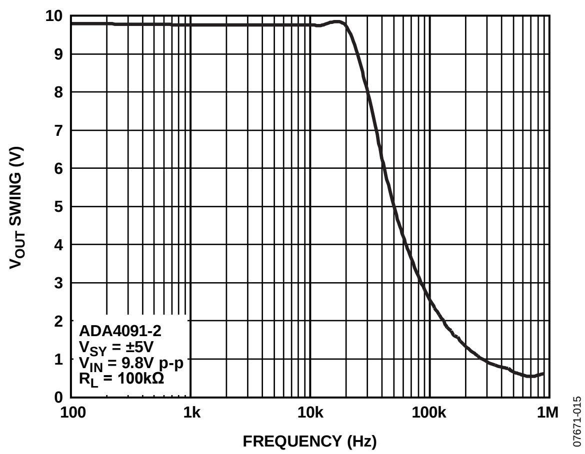


Figure 24. Output Voltage Swing vs. Frequency

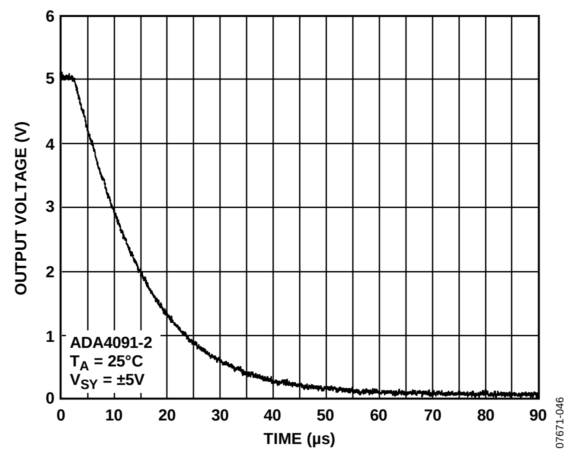


Figure 27. Positive Overload Recovery

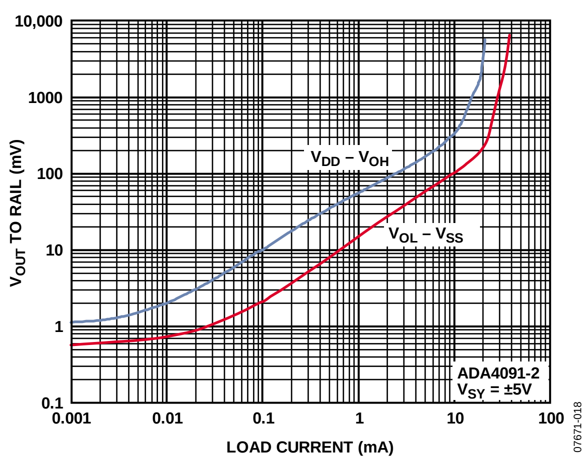


Figure 25. Dropout Voltage vs. Load Current

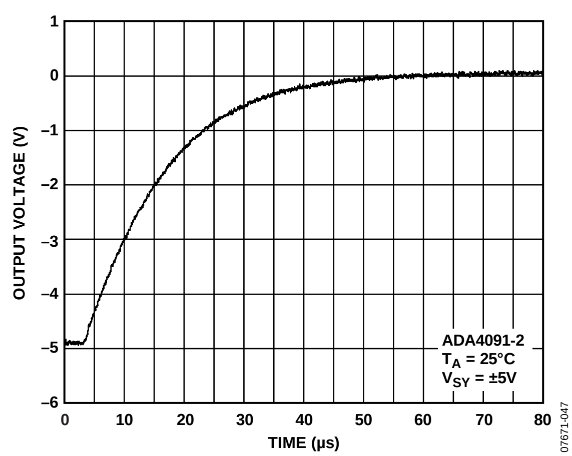


Figure 28. Negative Overload Recovery

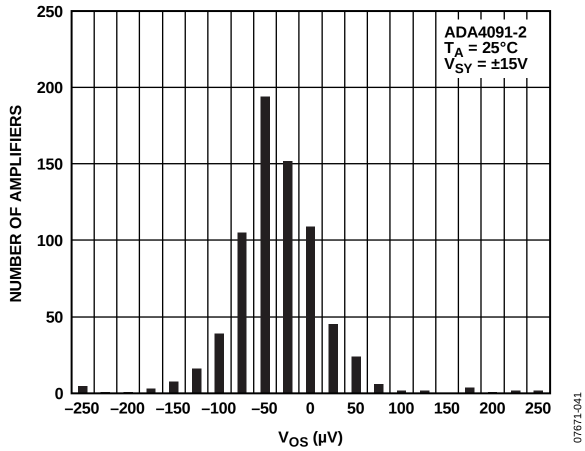


Figure 29. Input Offset Voltage Distribution

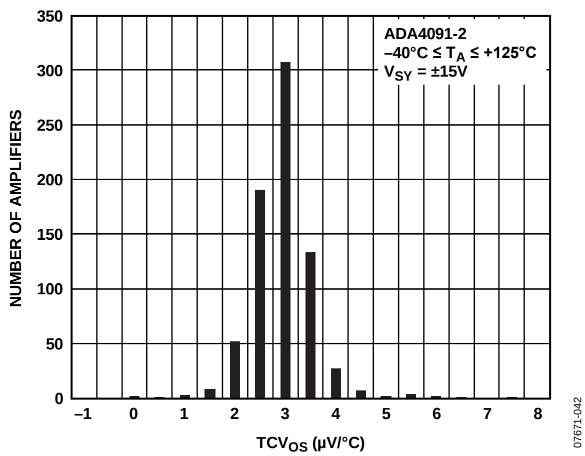


Figure 30. TCV_{OS} Distribution

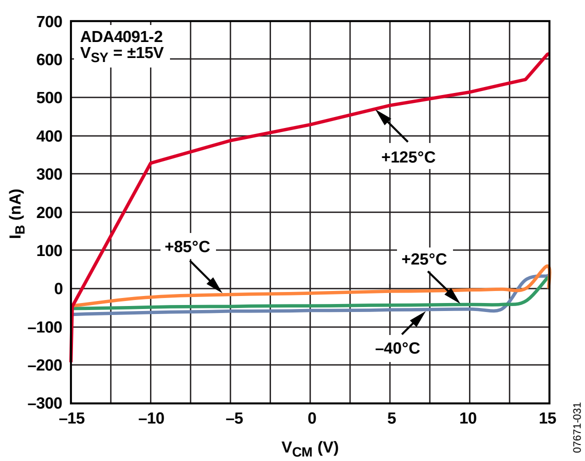


Figure 31. Input Bias Current vs. Common-Mode Voltage

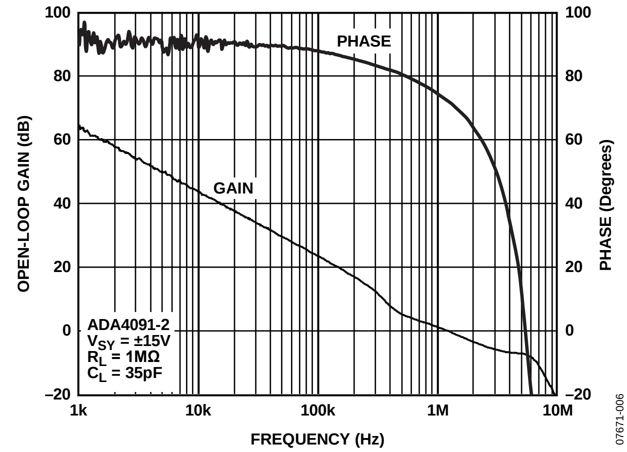


Figure 32. Open-Loop Gain and Phase vs. Frequency

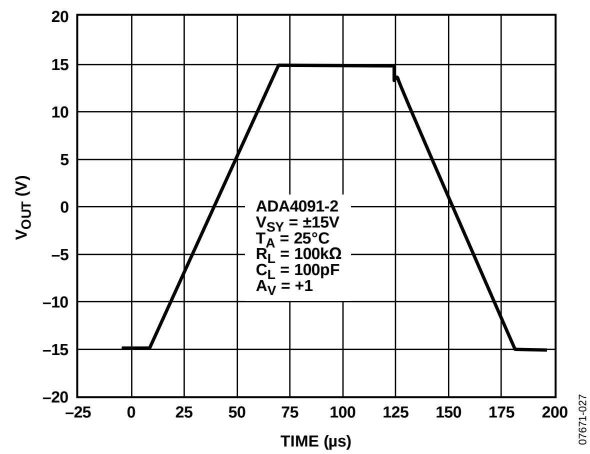


Figure 33. Large Signal Transient Response

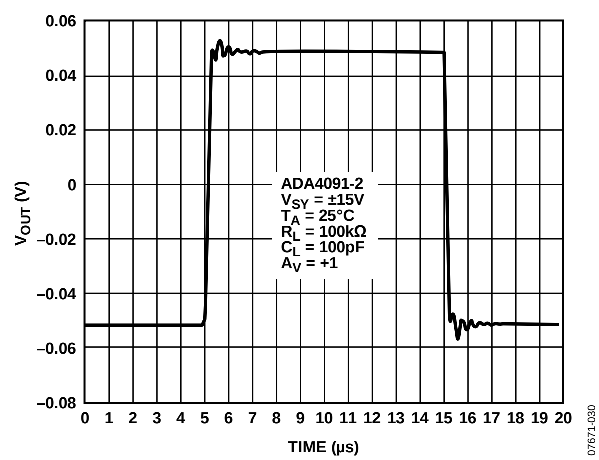


Figure 34. Small Signal Transient Response

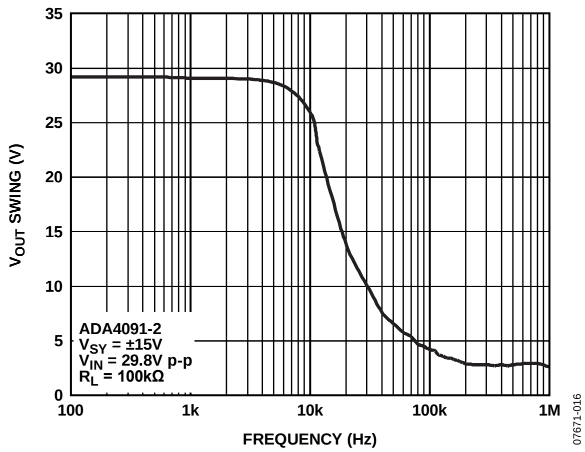


Figure 35. Output Voltage Swing vs. Frequency

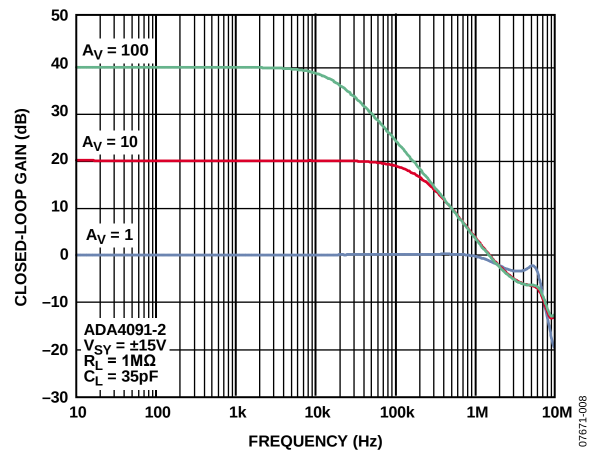


Figure 38. Closed-Loop Gain vs. Frequency

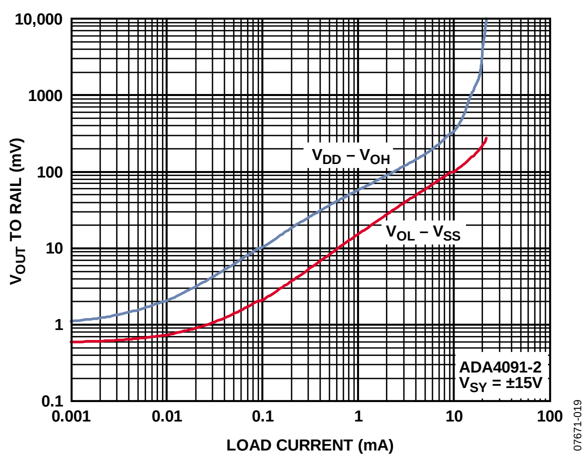


Figure 36. Dropout Voltage vs. Load Current

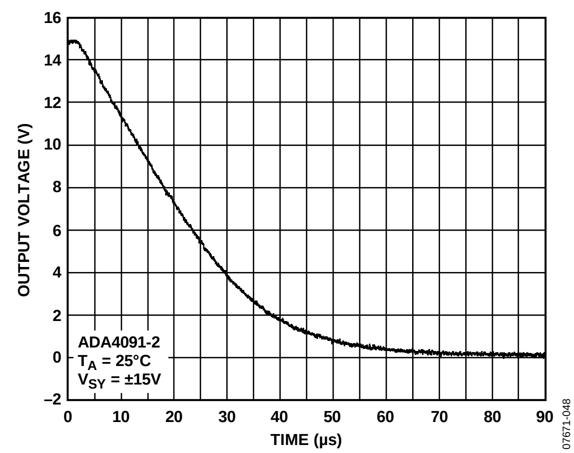


Figure 39. Positive Overload Recovery

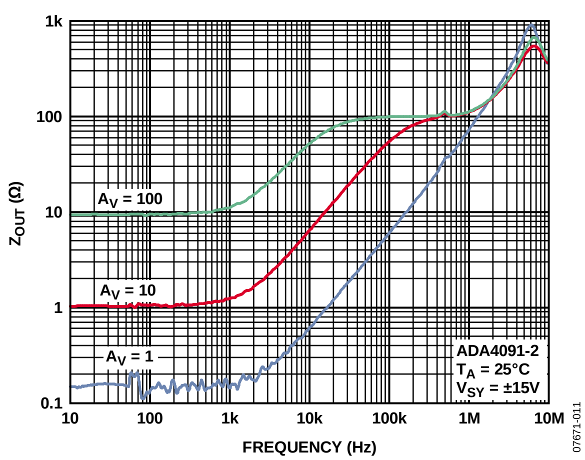


Figure 37. Output Impedance vs. Frequency

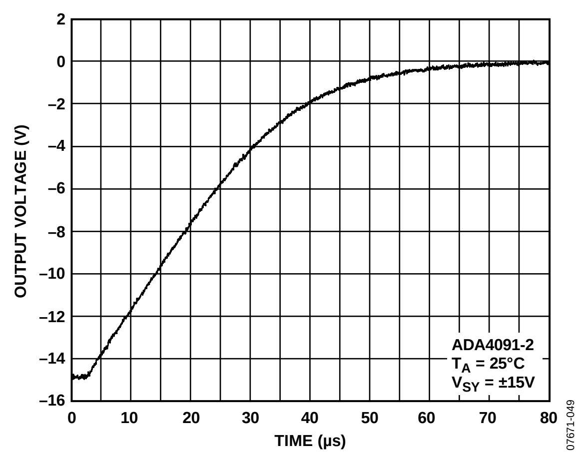


Figure 40. Negative Overload Recovery

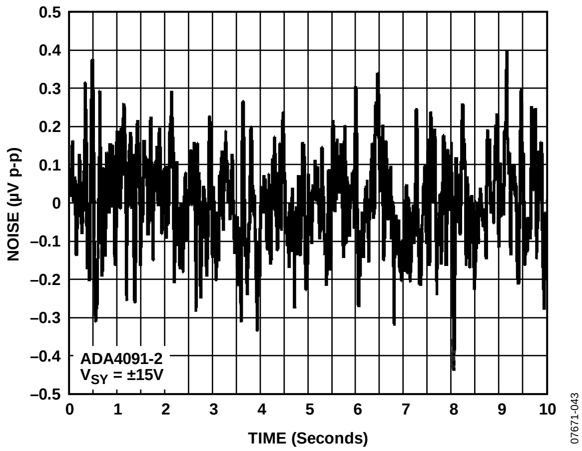


Figure 41.Peak-to-Peak Voltage Noise

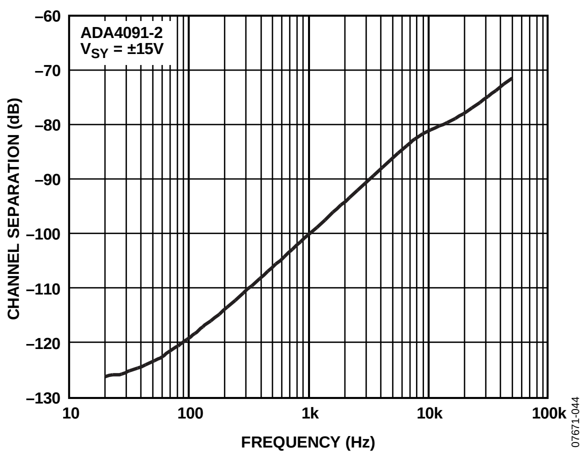


Figure 42. Channel Separation vs. Frequency

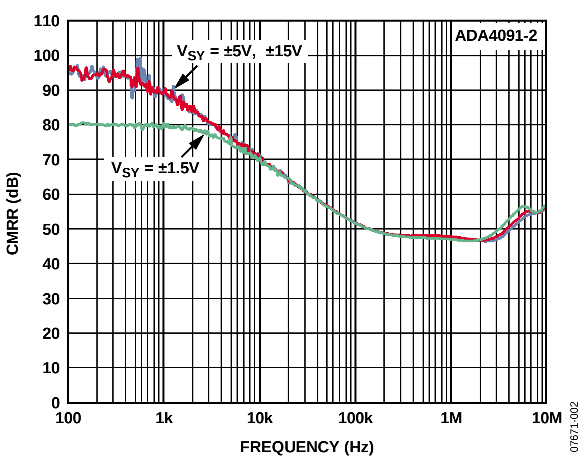


Figure 43. CMRR vs. Frequency

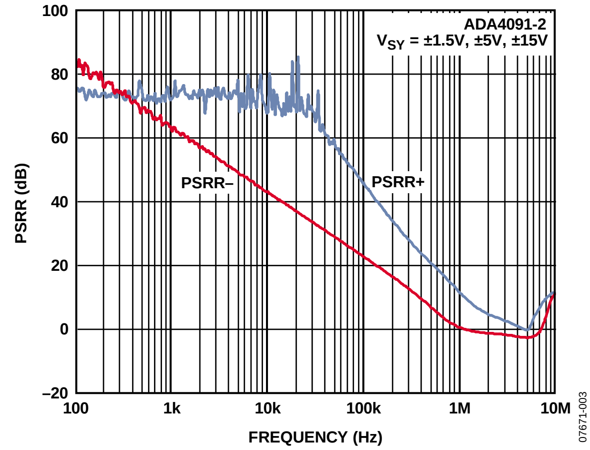


Figure 44. PSRR vs. Frequency

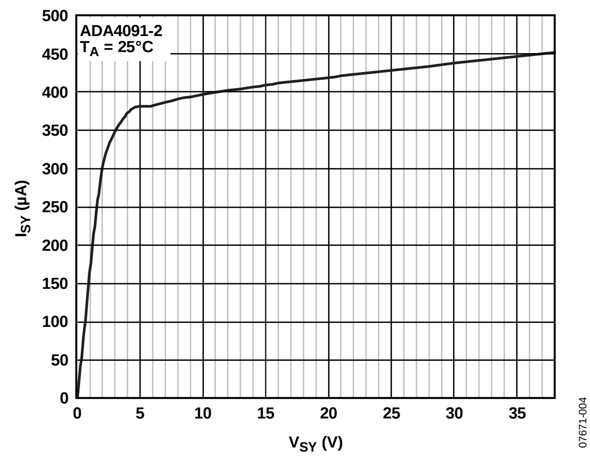


Figure 45. Supply Current vs. Supply Voltage

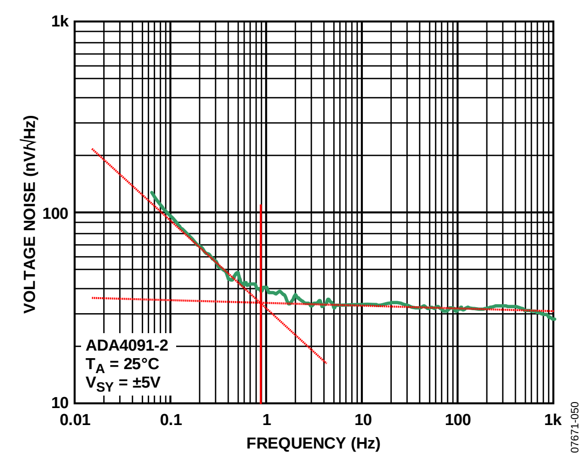


Figure 46. Voltage Noise Density

THEORY OF OPERATION

The ADA4091 family is a single-supply, micropower amplifier featuring rail-to-rail inputs and outputs. To achieve wide input and output ranges, these amplifiers employ unique input and output stages.

INPUT STAGE

In Figure 47, the input stage comprises two differential pairs, a PNP pair (PNP input stage) and an NPN pair (NPN input stage). These input stages do not work in parallel. Instead, only one stage is on for any given input common-mode signal level. The PNP stage (Transistor Q1 and Transistor Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. Alternatively, the NPN stage (Transistor Q5 and Transistor Q6) is needed for input voltages up to, and including, the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as shown in Figure 7, Figure 21, and Figure 31. Notice that the bias current switches direction at approximately 1.5 V below the positive rail. At voltages below this level, the bias current flows out of the ADA4091-x input, from the PNP input stage. Above this voltage, however, the bias current enters the device, due to the NPN stage. The actual mechanism within the amplifier for switching between the input stages comprises Transistor Q3, Transistor Q4, and Transistor Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually, the emitters of Q1 and Q2 are high enough to turn on Q3, which diverts the tail current away from the PNP input stage, turning it off. The tail current of the PNP pair is diverted to the Q4/Q7 current mirror to activate the NPN input stage.

A common practice in bipolar amplifiers to protect the input transistors from large differential voltages is to include series resistors and differential diodes. See Figure 48 for the full input protection circuitry. These diodes turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current flows between the input pins, limited only by the two 5 kΩ resistors. Evaluate each application carefully to make sure that the increase in current does not affect performance.

OUTPUT STAGE

The output stage in the ADA4091-x device uses a PNP and an NPN transistor, as do most output stages. However, Q32 and Q33, the output transistors, connect with their collectors to the output pin to achieve the rail-to-rail output swing.

As the output voltage approaches either the positive or negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage has inherent gain arising from the transistor output impedance, as well as any external load impedance; consequently, the open-loop gain of the op amp is dependent on the load resistance and decreases when the output voltage is close to either rail.

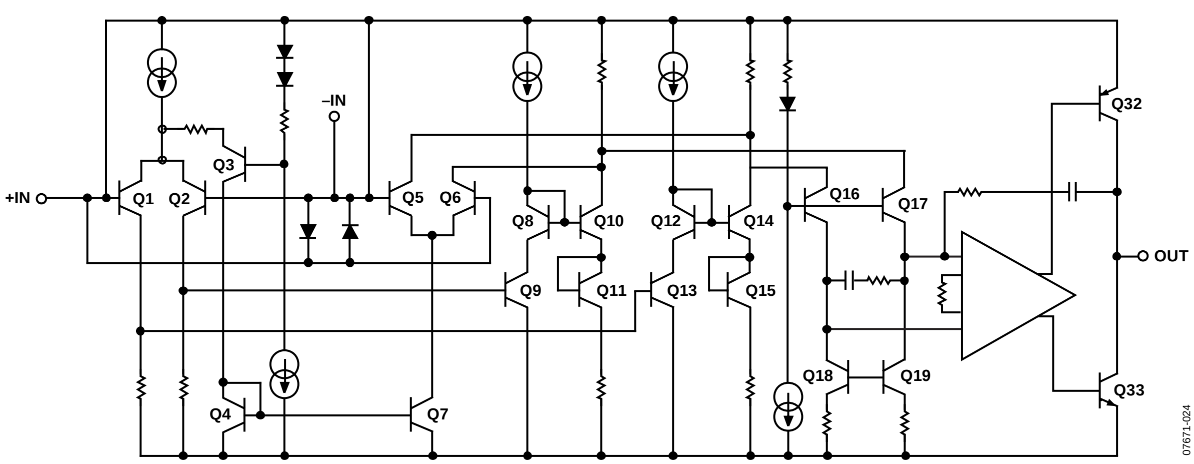


Figure 47. Simplified Schematic Without Input Protection (see Figure 48)

INPUT OVERVOLTAGE PROTECTION

The ADA4091-x has two different ESD circuits for enhanced protection, as shown in Figure 48.

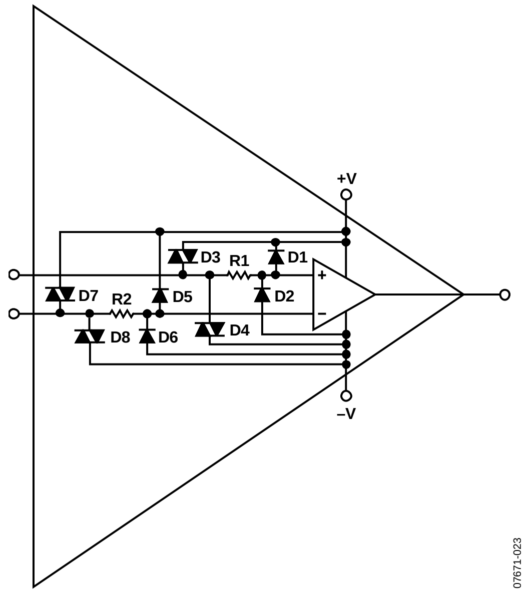


Figure 48. Complete Input Protection Network

One circuit is a series resistor of 5 kΩ to the internal inputs and diodes (D1 and D2 or D5 and D6) from the internal inputs to the supply rails. The other protection circuit is a circuit with two DIACs (D3 and D4 or D7 and D8) to the supply rails. A DIAC can be considered a bidirectional Zener diode with a transfer characteristic, as shown in Figure 49.

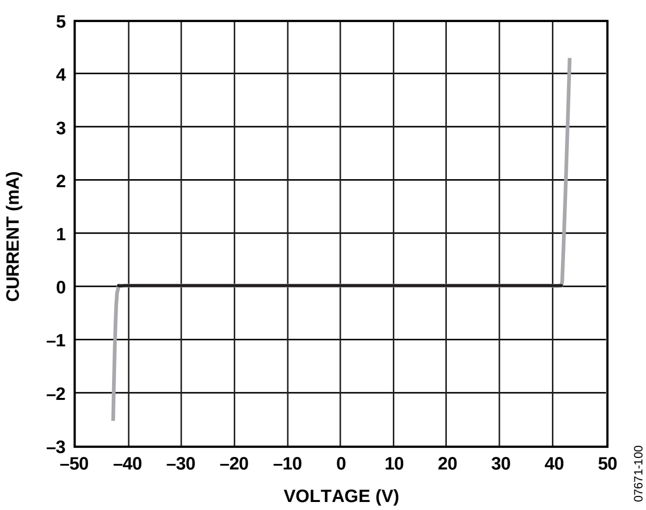


Figure 49. DIAC Transfer Characteristic

For a worst-case design analysis, consider two cases. The ADA4091-x has a normal ESD structure from the internal op amp inputs to the supply rails. In addition, it has 42 V DIACs from the external inputs to the rails, as shown in Figure 47.

Therefore, two conditions need to be considered to determine which case is the limiting factor.

- Condition 1. Consider, for example, that when operating on ±15 V, the inputs can go +42 V above the negative supply rail. With the −V pin equal to −15 V, +42 V above this supply (the negative supply) is +27 V.
- Condition 2. There is a restriction on the input current of 5 mA through a 5 kΩ resistor to the ESD structure to the positive rail. In Condition 1, +27 V through the 5 kΩ resistor to +15 V gives a current of 2.4 mA. Thus, the DIAC is the limiting factor. If the ADA4091-x supply voltages are changed to ±5 V, then −5 V + 42 V = +37 V. However, +5 V + (5 kΩ × 5 mA) = 30 V. Thus, the normal resistor diode structure is the limitation when running on lower supply voltages.

Additional resistance can be added externally in series with each input to protect against higher peak voltages; however, the additional thermal noise of the resistors must be considered.

The flatband voltage noise of the ADA4091-x is approximately 24 nV/√Hz, and a 5 kΩ resistor has a noise of 9 nV/√Hz. Adding an additional 5 kΩ resistor increases the total noise by less than 15% root sum square (rss). Therefore, maintain resistor values below this value (5 kΩ) when overall noise performance is critical.

Note that this represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2, Table 3, and Table 4.

OUTLINE DIMENSIONS

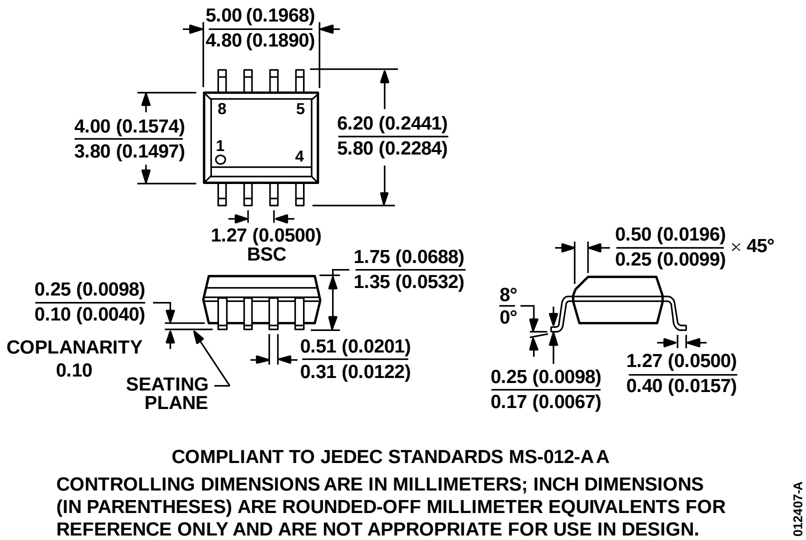


Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

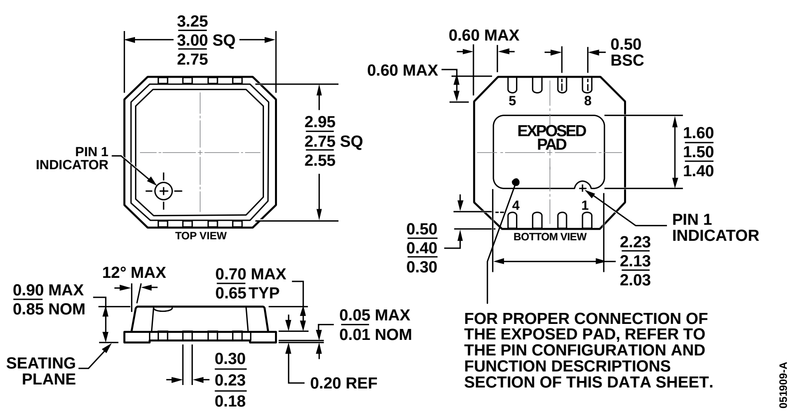


Figure 51. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-9)
Dimensions shown in millimeters

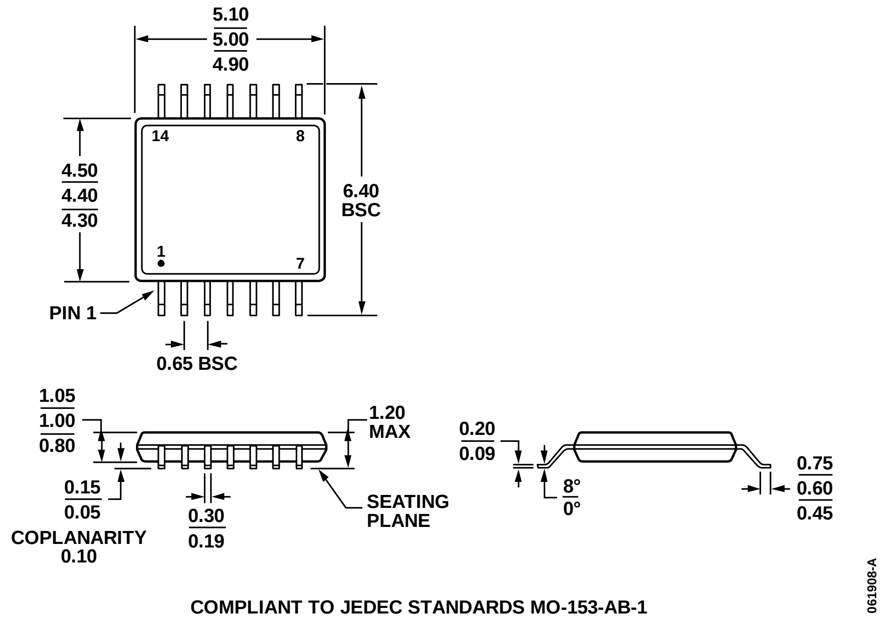


Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

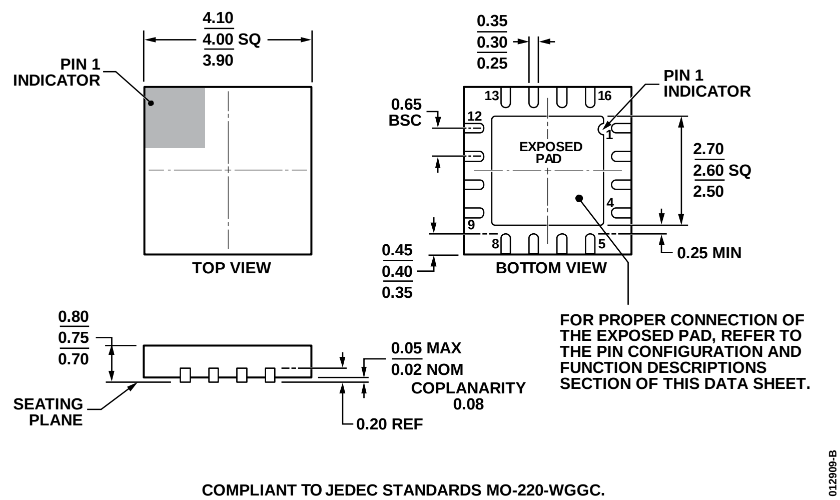


Figure 53. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-17)
Dimensions are millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4091-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADA4091-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADA4091-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADA4091-2ACPZ-R2	−40°C to +125°C	8-Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-9	A1Z
ADA4091-2ACPZ-R7	−40°C to +125°C	8-Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-9	A1Z
ADA4091-2ACPZ-RL	−40°C to +125°C	8-Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-9	A1Z
ADA4091-4ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	RU-14	
ADA4091-4ARUZ-RL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	RU-14	
ADA4091-4ACPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-17	
ADA4091-4ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-17	
ADA4091-4ACPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-17	

[1] Z = RoHS Compliant Part.

NOTES

NOTES